Data Sheet December 2001

-6A, -100V, 0.600 Ohm, P-Channel Power MOSFET

The 2N6896 is a P-Channel enhancement mode silicon gate power MOS field effect transistor designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high power bipolar switching transistors.

Ordering Information

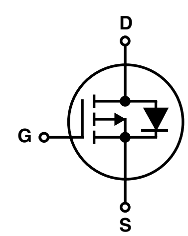
PART NUMBER	PACKAGE	BRAND
2N6896	TO-204AA	2N6896

NOTE: When ordering, include the entire part number.

Features

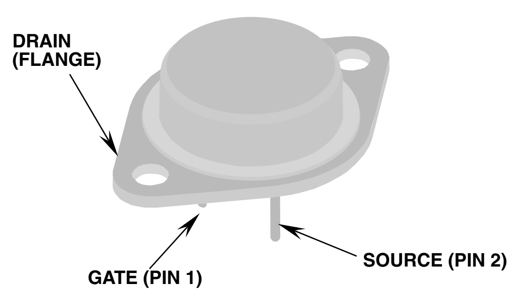
- -6A, -100V
- $r_{DS(ON)} = 0.600\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-204AA



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		2N6896	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	-100	V
Drain to Gate Voltage ($R_{GS} = 1M\Omega$) (Note 1)	V_{DGR}	-100	V
Continuous Drain Current	I_D	-6	A
Pulsed Drain Current	I_{DM}	-20	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	60	W
Above $T_C = 25^oC$, Derate Linearly		0.48	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 1mA$, $V_{GS} = 0V$	-100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 0.25mA$	-2	-	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80V$	-	-	1	μA
		$V_{DS} = -80V$, $T_C = 125^oC$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	-	100	nA
Drain to Source On-Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 3.8A$, $V_{GS} = -10V$	-	-	2.28	V
		$I_D = 6A$, $V_{GS} = -10V$	-	-	-6	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 3.8A$, $V_{GS} = -10V$	-	-	0.600	Ω
		$I_D = 3.8A$, $V_{GS} = 10V$, $T_C = 125^oC$	-	-	0.960	Ω
Forward Transconductance (Note 2)	g_{fs}	$I_D = 3.8A$, $V_{DS} = -10V$	1	-	4	S
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = -25V$ f = 0.1MHz	200	-	800	pF
Output Capacitance	C_{OSS}		100	-	350	pF
Reverse-Transfer Capacitance	C_{RSS}		40	-	150	pF
Turn-On Delay Time	$t_{d(ON)}$	$I_D = 3.8A$, $V_{DS} = -50V$ $R_{GEN} = R_{GS} = 15\Omega$, $V_{GS} = -10V$	-	-	60	ns
Rise Time	t_r		-	-	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	150	ns
Fall Time	t_f		-	-	100	ns
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	2.083	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 12A$	0.8	-	1.6	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 4A$, $dI_{SD}/dt = 50A/\mu s$	-	-	375	ns

NOTES:

2. Pulsed: Pulse duration = 300μs, max, duty cycle = 2%.
3. Repetitive Rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

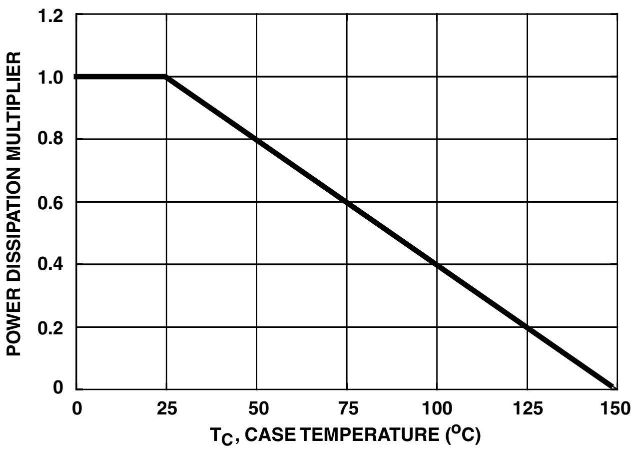


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

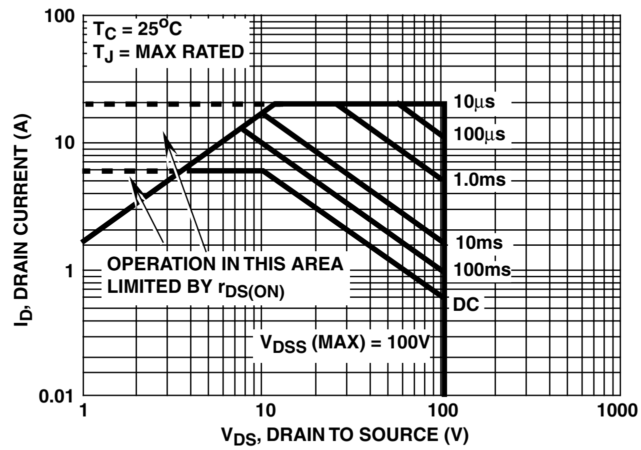


FIGURE 2. FORWARD BIAS OPERATING AREAS

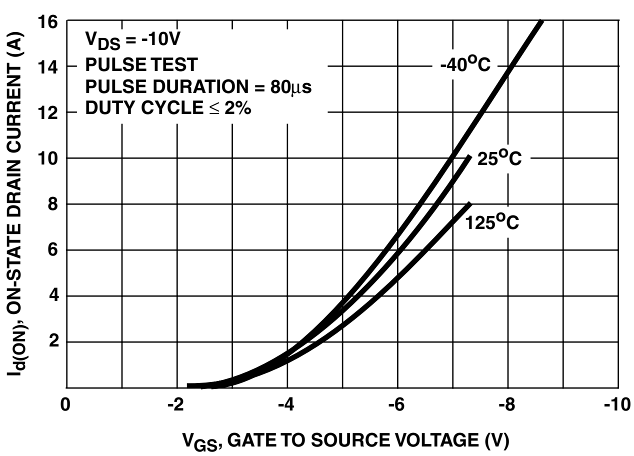


FIGURE 3. TRANSFER CHARACTERISTICS

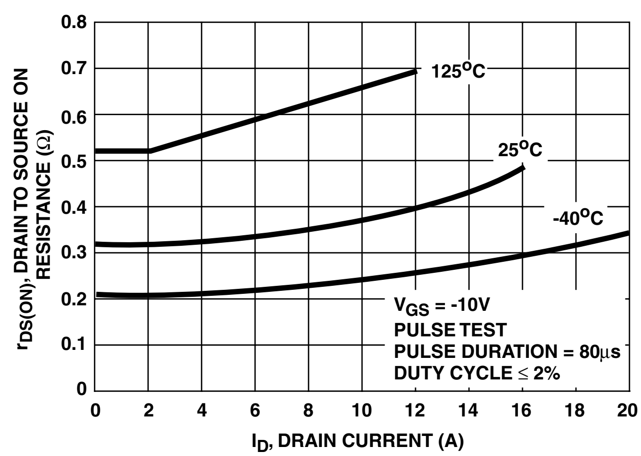


FIGURE 4. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

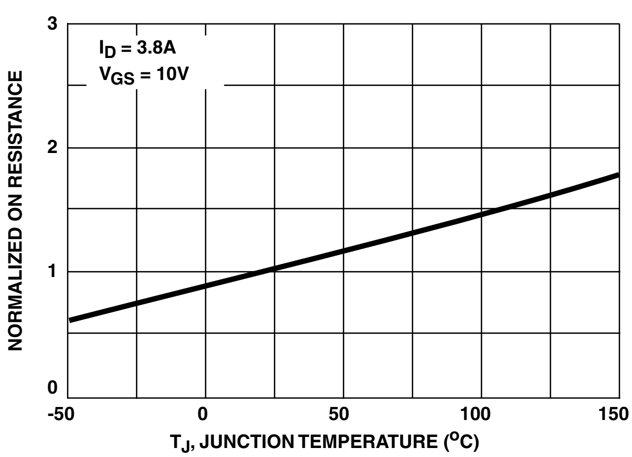


FIGURE 5. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

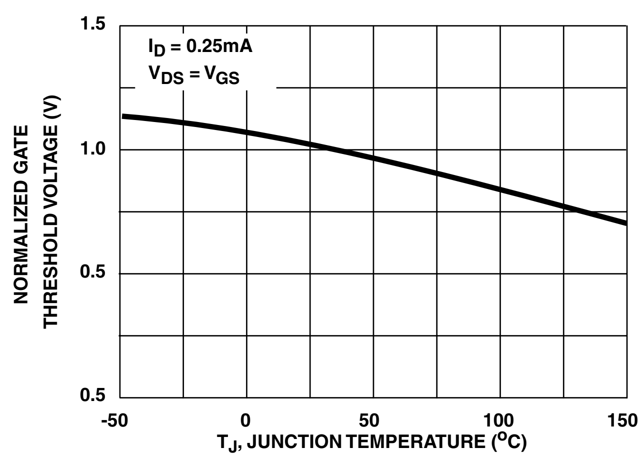


FIGURE 6. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

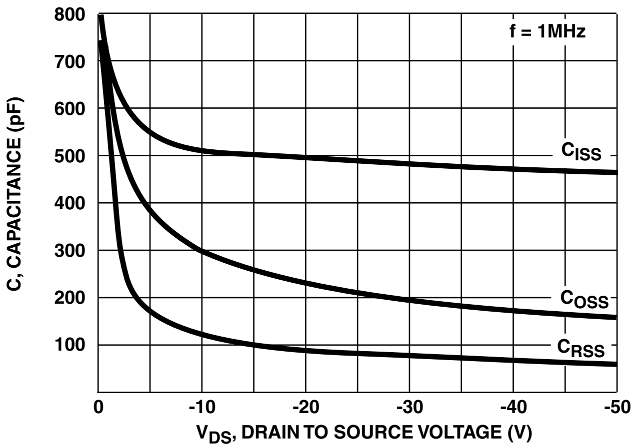


FIGURE 7. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

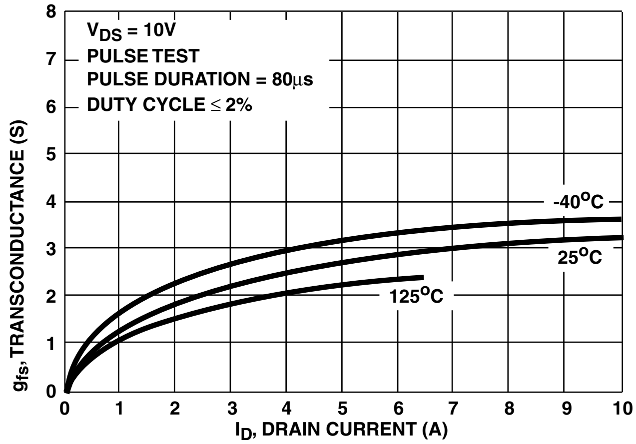


FIGURE 8. TRANSCONDUCTANCE vs DRAIN CURRENT

Test Circuits and Waveforms

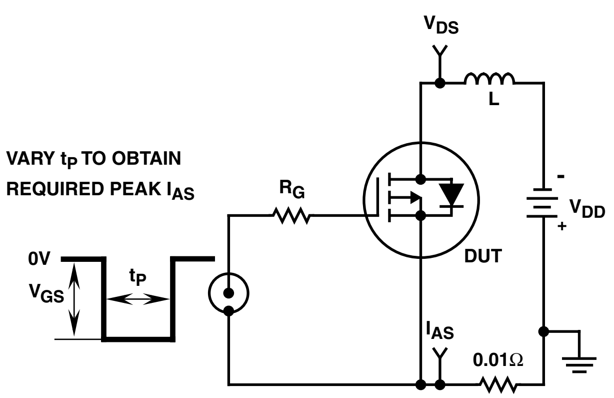


FIGURE 9. UNCLAMPED ENERGY TEST CIRCUIT

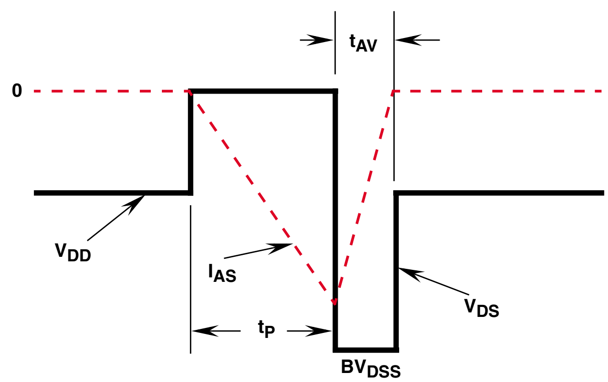


FIGURE 10. UNCLAMPED ENERGY WAVEFORMS

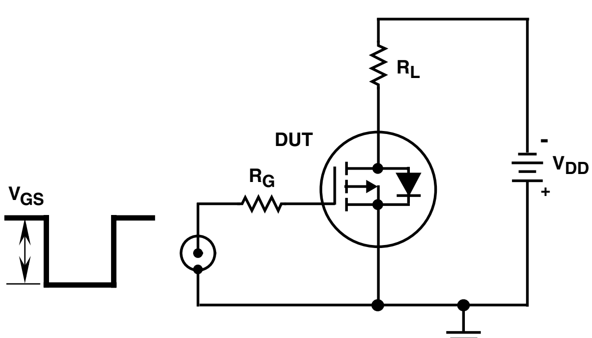


FIGURE 11. SWITCHING TIME TEST CIRCUIT

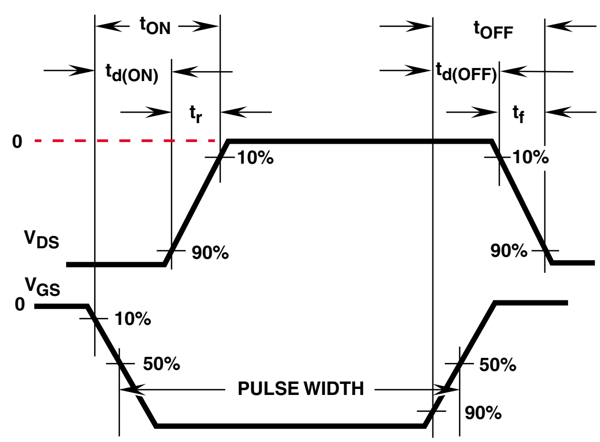


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

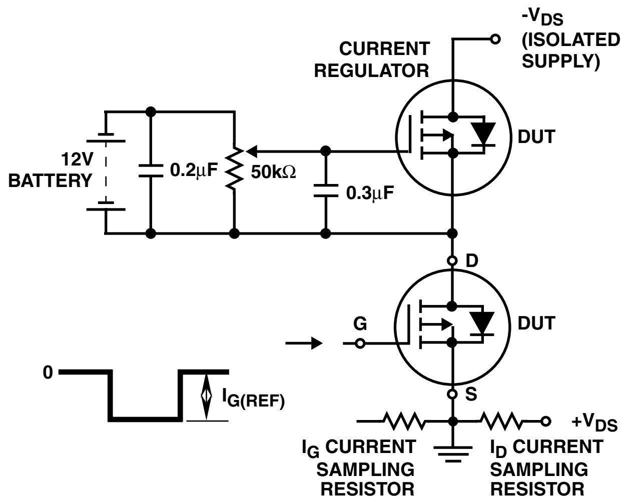


FIGURE 13. GATE CHARGE TEST CIRCUIT

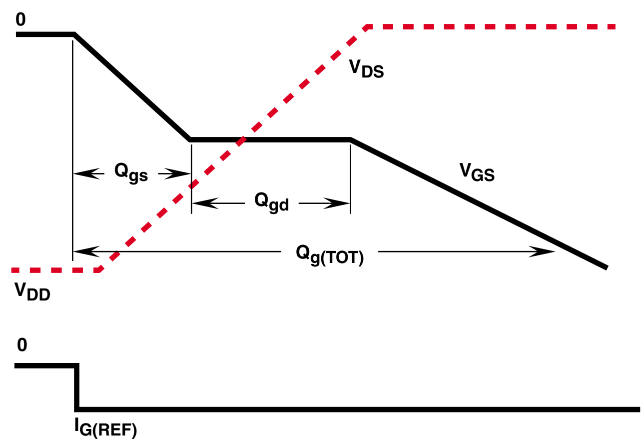


FIGURE 14. GATE CHARGE WAVEFORMS

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